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#16/Appeal Brief
6/3/03
C.P.

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR: Kirk D. Prall et al.

SERIAL NO.: 09/503,638 **GROUP ART UNIT:** 2814

FILED: February 14, 2000 **EXAMINER:** G. Peralta

TITLE: Random Access Memory

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SIR:

APPELLANTS'/APPLICANTS' OPENING BRIEF ON APPEAL

1. Real Party In Interest.

Micron Technology, Inc. owns this patent application.

2. Related Appeals And Interferences.

There are no other appeals or interferences known to Appellants, Appellants' legal representative or the Assignee which will affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

3. Status Of Claims.

Claims 23-28 and 30-33 are pending. Claims 1-22 and 29 have been canceled. All pending claims, Claims 23-28 and 30-33, are appealed.

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4. **STATUS OF AMENDMENTS.**

No amendments were filed after the final action.

5. **SUMMARY OF INVENTION.**

The claims are directed to devices that can be used to enhance refresh in random access memories. For example, the semiconductor memory device recited in Claim 23 includes a first dopant implant in a capacitor contact region and a bit line contact region (e.g., lightly doped source/drain regions 32A and 32B in Figs. 2-8) and a second dopant implant in only the capacitor contact region (e.g., the dotted lines in Figs. 3-8). Specification, page 9, line 11 through page 10, line13. In another example, the semiconductor memory device recited in Claim 30 includes first and second dopant implants in a contact region. The implant profile of the second dopant implant (e.g., the dotted lines in Figs. 3-8) is narrower and deeper than the implant profile of the first dopant implant (e.g., lightly doped source/drain regions 32A and 32B in Figs. 2-8). Specification, page 9, line 11 through page 10, line13.

6. **ISSUES.**

1. Does Katayama (U.S. Patent No. 5,444,278) disclose all of the limitations of Claims 23-24, 26-28 and 30-32 as required to support the Examiner's Section 102 rejection of those claims?

1(a). Does Katayama disclose two implants into the same contact region?

1(b). Has the Examiner offered any evidence to support the supposition that a diffusion layer is structurally identical to an implant?

7. **GROUPING OF CLAIMS.**

Applicant proposes the following grouping of claims according to the Issues noted above in Section 6.

Issue No. 1: Claims 23-28 and 30-33.

8. **ARGUMENT.**

ISSUE NO. 1

Katayama Does Not Disclose All Of The Limitations Of Claims 23-24, 26-28 And 30-32 As Required To Support The Section 102 Rejection Of Those Claims

Claims 23-24, 26-28 and 30-32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Katayama (U.S. Patent No. 5,444,278). A claim is anticipated only if each and every element in the claim is found expressly or inherently in the reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989).

Issue 1(a): Katayama does not disclose two implants into the same contact region as required by Claims 23-24, 26-28 and 30-32.

Claims 23-24 and 26-28 recite "a first dopant implant in the capacitor and bit line contact regions" and "a second dopant implant in only the capacitor contact region."[1] Claims 30-32 recite "a first dopant implant in the contact region" and "a second dopant implant in the contact region."

The Examiner incorrectly asserts that Katayama discloses "a second dopant implant 104 in only the capacitor contact region" (Office Action mailed 11/27/2002, page 2) and that "Katayama teaches the formation of the second impurity region by both diffusion and implantation, in col. 19, lines 55-67, it is taught that there is a second dopant implant only in the capacitor contact region" (Office Action mailed 11/27/2002, page 4.

The passage in Katayama cited by the Examiner describes two implants. However, only one of the implants (implantation layer 104) is in the contact region. Consistent with the other embodiments shown and described in Katayama, the embodiment in Fig. 36, which is described at col. 19, line 55 through col. 20, line 24, includes an implantation layer 104 and then a diffusion layer 105 formed at the region contacting capacitor lower electrode 112. A diffusion layer is not an implant, and the Examiner has made no specific assertion to the contrary. Katayama does

[1] Claim 28 actually recites "a second dopant implant in only the capacitor contact...." "Region" was inadvertently omitted from the second implant element of Claim 28 -- a mistake that was not discovered until now.

not teach two implants at the region contacting capacitor lower electrode 112. Therefore, Katayama does not anticipate any of Claims 23-24, 26-28 and 30-32.

Issue 1(b): The Examiner Has Not Offered Any Evidence To Support The Supposition That A Diffusion Layer Is Structurally Identical To An Implant.

The Examiner has not offered any evidence to support her supposition that the structures formed by diffusion and implantation are identical. At page 4 of the Office Action mailed 11/27/2002, the Examiner states that "the presence of process limitations on [sic] product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product." Although the Examiner does not explain how or why this statement supports the rejection, she is apparently supposing that a dopant implant is structurally identical to a dopant diffusion layer. Katayama repeatedly distinguishes implantation layers and diffusion layers -- implantation layer 3b and impurity diffusion layer 4 in Fig. 1, implantation layer 23b and diffusion layer 24 in Fig. 13 and implantation layer 104 and diffusion layer 105 in Fig. 36 to name just a few. Nothing in Katayama teaches or even suggests any of the implantation layers are structurally identical to any of the diffusion layers.

The Examiner carries the burden of establishing a prima facie case of anticipation with "specific fact findings for each contested limitation and satisfactory explanations for such findings." *Gechter v. Davidson,* 116 F.3d 1454, 43 USPQ 2d 1030, 1035 (Fed. Cir. 1997). The Examiner must produce evidence to support her supposition that diffusion layers and implants are the same thing, because Katayama clearly does not. Absent such evidence, the rejection should have been withdrawn.

Claims 25 and 33 were rejected under Section 103 as being obvious over Katayama. Claim 25 depends from Claim 24. Claim 33 depends from Claim 32. For the reasons noted above for the base claims, Claims 25 and 33 also distinguish patentably over Katayama.

Respectfully submitted,
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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

23. A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type; and

a second dopant implant in only the capacitor contact region.

24. A device according to Claim 23, wherein the second dopant implant is deeper than the first dopant implant.

25. A device according to Claim 24, wherein the depth of the first dopant implant is in the range of 500 angstroms to 1000 angstroms and the depth of the second dopant implant is up to 2,000 angstroms.

26. A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type;

insulating spacers extending along the sidewalls of the gate electrode and over a portion of the first dopant implant in the capacitor and bit line contact regions; and

a second dopant implant in only the capacitor contact region, the second dopant implant aligned with the insulating spacer extending over the capacitor contact region such that substantially all of the second dopant implant is formed in only that portion of the capacitor contact region not covered by the insulating spacer.

27. A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure having a first conductivity type;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type;

insulating spacers extending along the sidewalls of the gate electrode and over a portion of the first dopant implant in the capacitor and bit line contact regions;

a second dopant implant in only the capacitor contact region, the second dopant implant aligned with the insulating spacer extending over the capacitor contact region such that substantially all of the second dopant implant is formed in only that portion of the capacitor contact region not covered by the insulating spacer;

a capacitor first conductor in electrical contact with the capacitor contact region;

a dielectric over the capacitor first conductor; and

a capacitor second conductor over the dielectric.

28. A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type, and the first dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy in the range of 20 KeV to 100 KeV;

insulating spacers extending along the sidewalls of the gate electrode and over a portion of the first dopant implant in the capacitor and bit line contact regions;

a second dopant implant in only the capacitor contact, the second dopant implant having the second conductivity type, and the second dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy up to 200 KeV;

a capacitor first conductor in electrical contact with the capacitor contact region, the capacitor first conductor comprising polysilicon doped to the second conductivity type to a level in the range of 1×10^{19} to 1×10^{20} atoms per cubic centimeter;

a dielectric over the capacitor first conductor; and

a capacitor second conductor over the dielectric.

30. A semiconductor memory device, comprising:

a substrate;

a contact region in the substrate;

a first dopant implant in the contact region, the first implant defining a first implant profile; and

a second dopant implant in the contact region, the second implant defining a second implant profile narrower and deeper than the first implant profile.

31. A device according to Claim 30, wherein the first and second dopants have the same conductivity type.

32. A device according to Claim 31, further comprising a capacitor in electrical contact with the contact region.

33. A device according to Claim 32, wherein the depth of the first dopant implant is in the range of 500 angstroms to 1000 angstroms and the depth of the second dopant implant is up to 2,000 angstroms.